

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	61	behavior\$2 adj2 consistency	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 13:08
L2	31	language and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 13:11
L3	6	vector and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 13:11
S1	2	"20050071147"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 10:39
S2	1	unwinding with bound with language	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 10:47
S3	1	unwinding with loop with language	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 10:40
S4	13	unwinding with language	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 10:40
S5	154	unwinding with bound	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 10:48

## EAST Search History

S6	0	behavior\$ adj4 consisten\$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 10:50
S7	1566	behavior\$ adj4 consisten\$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 10:50
S8	9	behavior\$ adj4 consisten\$2 with language	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 10:51
S9	453625	vector	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 10:51
S10	2	S8 and S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/29 13:08



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1 [MINCE: Matching INstructions Using Combinational Equivalence for Extensible Processor](#)

Newton Cheung, Sri Parameswaran, Jörg Henkel, Jeremy Chan

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 2 DATE '04**

**Publisher:** IEEE Computer Society

Full text available: pdf(254.00 KB) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

Designing custom-extensible instructions for Extensible Processors<sup>1</sup> is a computationally complex task because of the large design space. The task of automatically matching candidate instructions in an application (e.g. written in a high-level language) to a pre-designed library of extensible instructions is especially challenging. Previous approaches have focused on identifying extensible instructions (e.g. through profiling), synthesizing extensible instructions, estimating expected performance ...

2 [Symbolic simulation and verification: Hardware verification using ANSI-C programs as a reference](#)

Edmund Clarke, Daniel Kroening

January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**

**Publisher:** ACM Press

Full text available: pdf(80.74 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

We describe an algorithm to verify a hardware design given in Verilog using an ANSI-C program as a specification. We use SAT based Bounded Model Checking [1] in order to reduce the equivalence problem to a bit vector logic decision problem. As a case study, we describe experimental results on a hardware and a software implementation of the data encryption standard (DES) algorithm.

3 [RTL-Datapath Verification using Integer Linear Programming](#)

Raik Brinkmann, Rolf Drechsler

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design ASP-DAC '02**

**Publisher:** IEEE Computer Society

Full text available: pdf(174.19 KB) Additional Information: [full citation](#), [abstract](#), [citations](#)

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Satisfiability of complex word-level formulas often arises as a problem in formal verification of hardware designs described at the register transfer level (RTL). Even though most designs are described in a hardware description language (HDL), like Verilog or VHDL, usually this problem is solved in the Boolean domain, using Boolean solvers. These engines often show a poor performance for data path verification. Instead of